Reduced-Size Cryocooler Electronics for Space

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ABSTRACT

Iris Technology has been performing research to reduce the size of cryocooler control electronics (CCE) for space-based missions during the last few years. In this presentation Iris Technology will explain the history, architecture, and performance of new single drive output and dual drive output, space based CCEs that Iris Technology began delivering this year.

INTRODUCTION

Iris has a long history of designing and developing cryocooler control electronics (CCEs). Recently Iris made efforts to advance the state-of-the art in CCEs by introducing new innovations utilizing the latest available space grade parts. These innovations have added two smaller CCEs, equivalent in performance to devices already in the Iris Technology product line

These new CCEs are smaller than the CCEs they replace and retain all of the performance of the original CCE. In some cases, the new offering adds an expanded feature set compared to the original. The CCEs are the µLCCE (rebranded as the ICE-G1-30) and the ICE-G2 (rebranded as the ICE-G2-100) which are 30 watt and 100 watt CCEs respectively.

FIRST TARGET - MLCCE

mLCCE to µLCCE

The first target in this size reduction campaign was the mLCCE. The mLCCE is a successful product used in the Small Sat community with the following features:

- Single 30-watt output power.
- Temperature control loop.
- Fits on one face of a 1U CubeSat.
- RS-422 Command and Control.

The µLCCE is a reduced size version of the mLCCE as shown in Figure 1. Size reduction, while maintaining performance and space worthiness were the primary goals for this set of control electronics. Size reduction targets were principally in three areas of the design:

- Power Conversion Circuits.
- System Processing Circuits.
- Signal Sensing Circuits.

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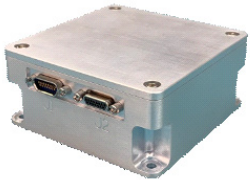
mLCCE (9.1 x 9.1 x 3.4 cm)
288 cm³



µLCCE (7.9 x 7.9 x 3.1 cm)
195 cm³

Figure 1. The mLCCE shown of the left is the predecessor to the μLCCE shown of the right. The μLCCE shown a significant size reduction (> 30%) while maintaining the same performance.

Size reductions were achieved by leveraging newly available components applied to these design areas.

As mentioned earlier, three design areas were targeted for reduction. The first was the output power conversion circuits. They were redesigned from a MOS FET design to a GaN FET design. While the FETs themselves are similar in size, moving 100 kHz to 500 kHz switching speeds allowed a reduction in the size of the associated passive components, mostly capacitors and inductors. The next target area was the system processing circuits. Here, the FPGA based design was replaced by a microcontroller-based design. This resulted in a smaller footprint with lower quiescent power. The last area targeted was the signal sensing circuits. Since the microcontroller has a built-in analog-to-digital converter (ADC) there was no need to include a discrete ADC in the design which saved additional power and size while reducing internal signal traces. Overall, this resulted in a 28% savings in board area and a 32% savings in volume. This is shown in Figure 1 and Figure 2.

NEXT TARGET – LCCE

LCCE to ICE-G2

The next target in this size reduction campaign was the LCCE. The LCCE is a TRL 9 product that was the first Iris developed CCE to be launched and is still orbiting. The LCCE is a dual

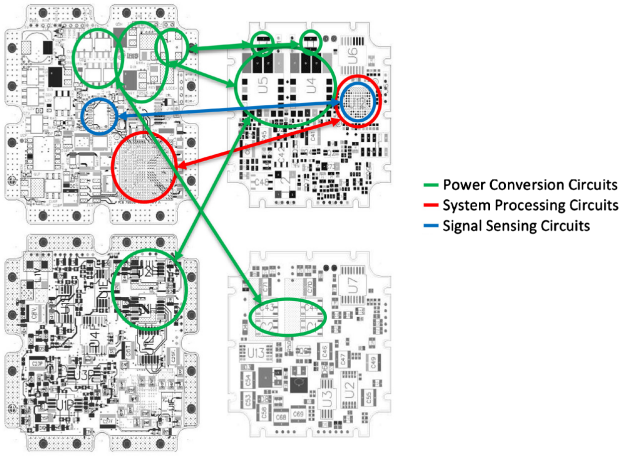


Figure 2. The larger board layout on the left is the top and bottom of the mLCCE. The smaller board layout on the right is the top and bottom of the μLCCE. The areas highlighted by the green circles are the output power conversion circuits, the areas highlighted by the red circles are the system processing circuits and the areas highlighted by the blue circles are the signal sensing circuits. This figure illustrates how the board area size reductions were accomplished.

Figure 3. The LCCE shown on the left is the predecessor to the ICE-G2 shown on the right. The ICE-G2 shows a significant size reduction (> 20%) while maintaining the same basic performance with additional performance enhancements.

50 Watt output power (total 100 Watts) CCE which has a temperature control loop and a RS-422 command and control interface. The LCCE is shown in Figure 3.

The ICE-G2 is a reduced size version of the LCCE with several enhancements. Size reduction while maintaining performance, space worthiness and enhanced performance were the primary goals for this set of control electronics. The same three design areas as the µLCCE were targeted for size reduction. Further enhancements were achieved through firmware and software

The ICE-G2 inherits all of the LCCE performance and includes:

- Multi-CCE communication (master/peripheral).
- Multi-CCE output waveform synchronization (w/ arbitrary phase).
- Active vibration control (across multiple CCEs).
- Reprogrammable software.

Major changes from LCCE are as follows:

- Power output drives changed from MOSFET to GaN FET and reduced the size of the power drives.
- Logic control changes from FPGA to microcontroller/FPGA, the FPGA added to µLCCE architecture to support second output drive as the microcontroller does not have enough PWM channels.
- Master/peripheral communication added to support multi-CCE synchronous operation.
- Accelerometer interface (inherited from LCCE2/HPLCCE2) was added to support active vibration control.
- Active vibration control algorithm expanded to multiple CCEs.
- Reprogrammable software allows customization to unique mission needs.

A block diagram of the ICE-G2 is shown in Figure 4.

ICE-G2 Performance

Since the ICE-G2 is being prepared for flight, there is measured performance data available. The first parameter verified was the power efficiency. The results are as follows:

- The ICE-G2 measures 89.7% at 85 W out.
- ICE-G2 can output power up to 100 watts.
- The efficiency at 100 watts is 90%.
- Gate drive efficiency is 93%.

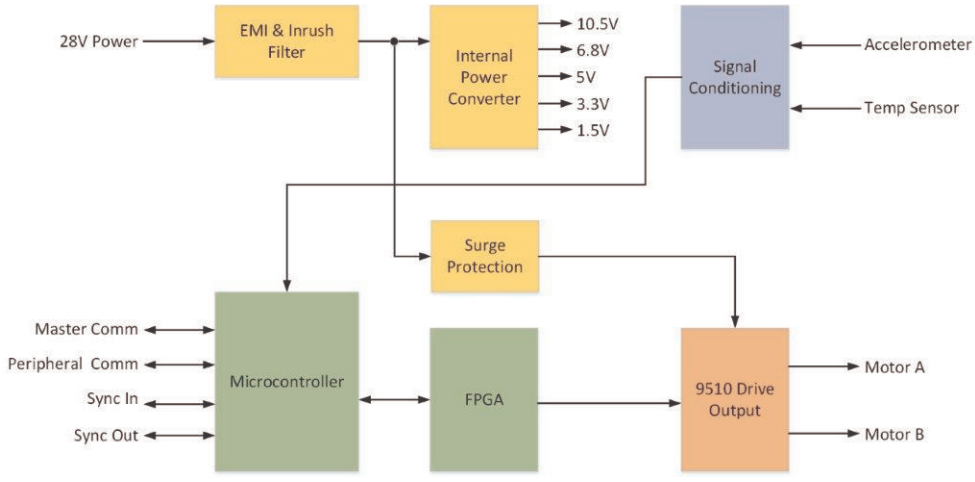


Figure 4. The ICE-G2 block diagram highlights the features and interfaces of this new CCE.

These results are better than the LCCE which was 85% at 100 watts. The efficiency plot is shown in Figure 5.

The next measured parameter is the active vibration cancellation performance. The ICE-G2 incorporates Iris Technologies' (patent pending) vibration cancellation algorithm, this algorithm can significantly reduce the vibration in the axis of piston motion. Testing was performed using a Thales LPT9510 mounted to an aluminum plate sitting on a laboratory bench. The results are shown in Figure 6. In the figure, before and after vibration is shown in both the time and frequency domains. These plots are based on data collected by the ICE-G2 and validated with an independent accelerometer system.

The data in Figure 6 demonstrates a vibration reduction of better than a factor of 10 in both time and frequency domains. The algorithm is capable of reducing the signal by larger factors given the right conditions. Experience has shown that this algorithm can push the vibration to the noise floor. This means that the vibration algorithm performance is primarily limited by the signal to noise ratio of the signal from the accelerometer. Because of this, Iris has taken special care to ensure signal integrity of the accelerometer signal. The accelerometer is a piezoelectric device that generates a charge signal in pico-coulombs. This requires careful design of the amplifier chain to ensure that the signal at the ADC is truly representative of the vibration signal with no additional noise added.

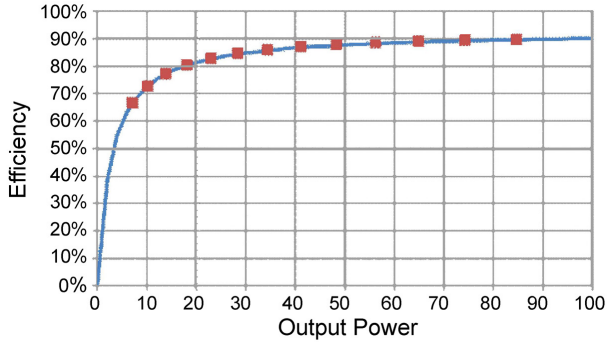


Figure 5. A measured efficiency plot from ICE-G2 testing. 90% efficiency is achieved at 100 watts of output power.

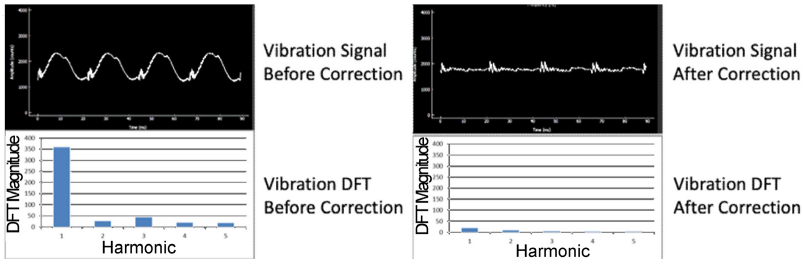


Figure 6. The ICE-G2 block diagram highlights the features and interfaces of this new CCE.

WHAT'S NEXT?

Iris Technology is continuing to evolve our CCE offerings. Both the µLCCE (ICE-G1-30) and the ICE-G2 (ICE-G2-100) have paths planned to evolve to more capable CCE offerings. These will be discussed in the following paragraphs. The basic architecture of both CCEs can be scaled to designs with different requirements such as different output power, input ripple filter, and launch locks. The building blocks for each of these functions is available from other Iris CCE developments.

µLCCE to HVM3 CCE

JPL has asked Iris to develop a modified µLCCE that includes:

- Input Ripple Filter
- Launch Locks

Iris designed a daughter board to accommodate these additional features. A clamshell mechanical design holds the new card as shown in Figure 7. The clamshell design allows the new daughter board to be mounted to the top half of the clamshell allowing this to replace the previous µLCCE chassis lid. This permits the reuse of the existing µLCCE chassis and board with only additional wires to make interconnects between the boards.

ICE-G2 to ICE-G2-100IL CCE

Based on the HVM3 CCE and the continuing effort at Iris to provide a configurable CCE, Iris is pursuing a new 100-watt CCE design that can optionally include an IRF and/or launch locks.

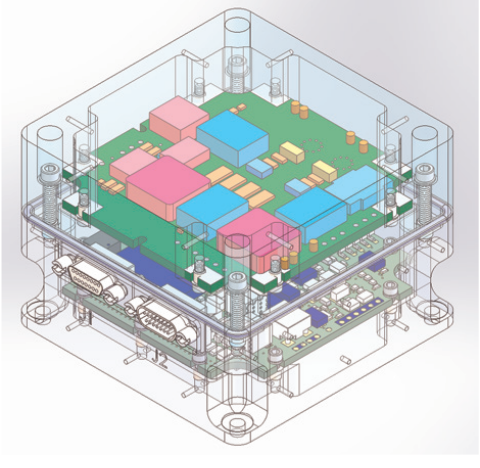


Figure 7. HVM3 CCE mechanical drawing. This design adds IRF and launch lock capabilities to the µLCCE.

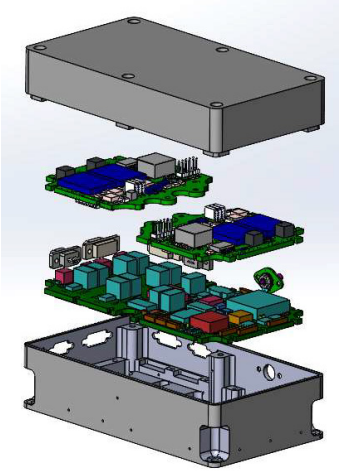


Figure 8. ICE-G2-100IL concept art. This concept adds optional IRF and launch lock capabilities to the ICE-G2 architecture.

This concept utilizes HVM3 mechanical clamshell concept and adds IRF and launch locks as two independent daughter boards. This allows either function to be added without the other. Like HVMS, this concept uses the top clamshell to hold the IRF and launch lock daughter boards, either one of which could be mounted separately. The bottom clamshell is the ICE-G2 with added wiring to connect to the additional functionality. An artist rendering of this concept is shown in Figure 8. In addition to IRF and launch locks, Iris is considering the feasibility of adding an optional power isolation daughter board for platforms which need power isolation.

ICE-G2 Potential Enhancements

The ICE-G2 architecture supports software re-programmability which allows customization of CCE operation for unique mission requirements. Iris would like to make the ICE-G2 re-programmable over its data interface which would allow on-orbit re-programmability to modify CCE characteristics after the system has launched, another enhancement being considered is fully digital power conversion. The current on-board power conversion single-ended primary-inductor converter (SEPIC) is a mostly analog design. Iris would like to design a digitally controlled converter which would be more size and power efficient and could be performed using digital control.

Iris Control Electronics History/Future

Iris Technology has a rich history of delivering flight CCEs. Figure 9 illustrates this history and shows selected future developments. This figure shows CCEs with output power between 30 and 800 watts.

CONCLUSIONS

Iris Technology has developed two new CCE architectures that are smaller and more robust than current generation CCEs. These new CCEs have led to a new configurable CCE concept that is being implemented for the HVM3 program. These new architectures and configurability is extensible to our entire line of CCEs from 30 to 800 watts

ACKNOWLEDGMENT

Iris Technology would like to thank Dean Johnson and the Jet Propulsion Laboratory (JPL) for their support on the HVM3 development.

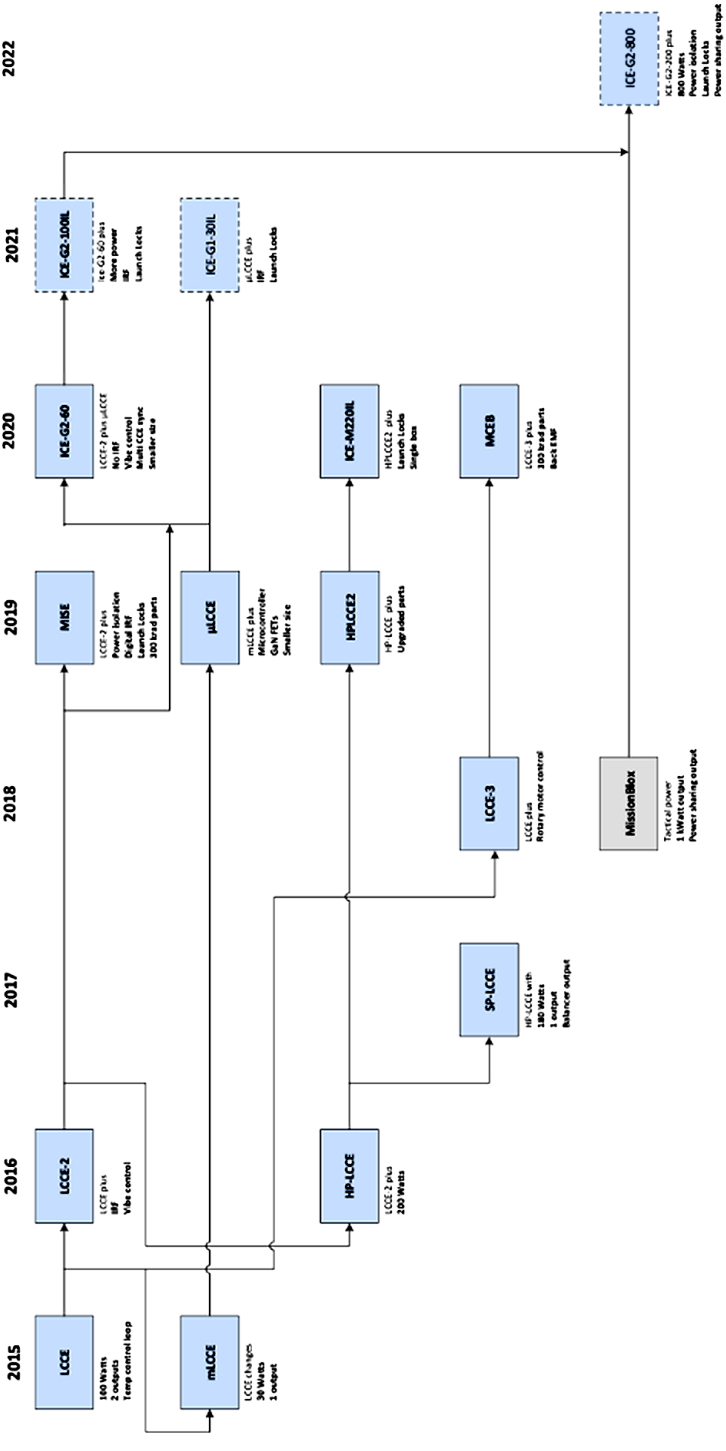


Figure 9. The ICE-G2 block diagram highlights the features and interfaces of this new CCE.